Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALAN DAVID BERENBAUM, NEVIN HEINTZE,
TOR E. JEREMIASSEN, and STEFANOS KAXIRAS

Appeal No. 2005-0492
Application No. 09/538,755

ON BRIEF

Before KRASS, BLANKENSHIP, and SAADAT Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-16, which are all of the claims pending in this application.

We reverse.

BACKGROUND

Appellants' invention relates to multithreaded processing using instruction packet splitting for greater utilization of hardware in very large instruction word processors. An

understanding of the invention can be derived from a reading of exemplary independent claim 1, which is reproduced as follows:

> 1. A multithreaded very large instruction word processor, comprising:
>
> a plurality of functional units for executing instructions from a multithreaded instruction stream, said instructions being grouped into instruction packets by a compiler; and
>
> an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator assigning instructions from at least one of said instruction packets to a plurality of said functional units, wherein said functional units can be allocated independently to any thread in said multithreaded instruction stream.

The following references are relied on by the Examiner:

Chung et al. (Chung)	5,404,469	Apr. 4, 1995
Keckler et al. (Keckler)	5,574,939	Nov. 12, 1996

Claims 1, 2, 6-9 and 13-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the disclosure of Chung.

Claims 1-5, 8-12, 15 and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Keckler.

We make reference to the answer (Paper No. 12, mailed March 31, 2004) for the Examiner's reasoning, and to the brief (Paper No. 11, filed March 11, 2004) and the reply brief (Paper No. 13, filed May 27, 2004) for Appellants' arguments thereagainst.

OPINION

With respect to the 35 U.S.C. § 102 rejection of claims 1, 2, 6-9 and 13-16 over Chung, Appellants argue that Chung does not allocate the instructions independently of the type of the instruction ready for execution within each thread (brief, page 3). Referring to the description of the four functional units in Chung (described as elements FU1, FU2, FU3 and FU4 in col. 7, lines 43-46), Appellants point out that each functional unit is dedicated to executing a particular type of instructions (id.). Appellants further conclude that each functional unit can be allocated to a thread that has an instruction ready only when the instruction type matches the capability of the functional unit (id.).

In response to Appellants' arguments, the Examiner mainly asserts that the claims do not require that the instructions be allocated independently of the type of instruction that is ready for execution (answer, page 3). In particular, the Examiner relies on Figure 8 and page 6 of Appellants' specification for describing that the functional units are not all assigned to one packet, but may be split across packets and different threads as the meaning for the phrase "allocated independently to any thread" (answer, page 4).

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

We observe that Chung does compile instruction threads in an interleaved manner (col. 7, lines 34-39) wherein each of the functional units FU1-FU4 receives instructions from its corresponding thread according to their type of instruction (col. 7, lines 40-53). Therefore, as argued by Appellants, each functional unit receives instructions only from the thread that matches the type of unit it is allocated to. Although it may be reasonable to argue that the claims do not recite the allocation of the functional units independent of the type of instructions, the claims do recite the allocation of the functional units "independently to any thread" which means no limitation on which

thread each functional unit corresponds to. In that regard, the functional units of Chung cannot be allocated independently to any thread in the instruction stream since they are limited in the kind of operations they perform and must receive instructions only from their corresponding thread.

In view of the discussion above, we find that the Examiner has failed to meet the burden of providing a prima facie case of anticipation with respect to claim 1 and claims 8, 15 and 16, which recite features similar to those of claim 1. Accordingly, the 35 U.S.C. § 102 rejection of claims 1, 2, 6-9 and 13-16 over Chung cannot be sustained.

Turning now to the 35 U.S.C. § 102 rejection of claims 1-5, 8-12, 15 and 16 over Keckler, we note that Appellants assert the same deficiency with the teachings of Keckler. In Particular, Appellants refer to Figure 1 of Keckler and argue that some of the operations from multiple threads have to be delayed due to functional unit conflict (brief, page 3). Appellants further point out that the functional units of Keckler could not be allocated independently to any thread since operations A3 and A4, for example, are locked out while their corresponding functional units are unavailable although other available functional units are present (id.). The Examiner, however, does not separately respond to the arguments regarding the rejection over Keckler and

appears to have intended the arguments related to Chung apply to both references.

We observe that Keckler, in Figure 1, shows allocation of the available functional units to the instructions from threads A-C where, similar to Chung, each functional unit receives instructions only from its corresponding thread. Therefore, when instructions from threads A and C compete for the same functional unit, one instruction has to be delayed even though other functional units may be available, but do not correspond to that particular thread (col. 4, lines 1-8).

In view of the discussion above, we find that the claimed allocation of functional units "independently to any thread in said multithreaded instruction stream" is absent in the interleaved processing scheme of Keckler. Accordingly, since the Examiner has failed to meet the burden of providing a prima facie case of anticipation, the 35 U.S.C. § 102 rejection of claims 1-5, 8-12, 15 and 16 over Keckler cannot be sustained.

OTHER ISSUES

In view of our decision herein, we recommend the Examiner consider provisionally rejecting claims 1-16 of this application under obviousness-type double patenting over the claims in the copending Application No. 09/538,670, alone or in combination with other prior art.

CONCLUSION

In view of the foregoing, the decision of the Examiner to reject claims 1-16 under 35 U.S.C. § 102 is reversed.

REVERSED

ERROL A. KRASS
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

MDS/ki

Appeal No. 2005-0492
Application No. 09/538,755

Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06430